Smalltalk Debug Lives in the Matrix

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What Matrix?

+ "Flexible" hardware
  Time to market

Hard to program
Hard to debug

Compute node

LUT LUT
LUT LUT
LUT LUT
LUT

µP

E/S

Programmable interconnection
What Matrix?

+ “Flexible” hardware
  Time to market

- Hard to program
  Hard to debug

Specific languages
Specific tools

Performances still
requires manual
tuning

EE skills required
State of the art debugging

Simplifying Xilinx and Altera FPGA Debug

Huge challenge

Debug Your FPGA Design At Full Speed

Solutions such as FPGAvi™ enable you to instantly move probe points within your Xilinx and Altera FPGAs without the need to recompile your design. Plus the ability to correlate internal FPGA signal activity to board-level signals can make the difference between hitting your schedule and missing your time-to-market window.
State of the art debugging

Touching the void

Simplifying Xilinx and Altera

Huge challenge

Meet in the middle
Debug silver bullet

- Observability
- Controlability
- Abstract analysis
- Fast changes

- Time to market
- Multiple runs
- Long cycles
- Simulation is not enough
Debug silver bullet

- Observability
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- Time to market
- Multiple runs
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New challenges: Threat or opportunity?
Operate at-speed

Keep your speed-up alive

Multiple runs prohibit any over time penalty
Operate in-situ

Because only HW brings speed-up

Debug requires extra circuitry
Debugging facilities are circuits
Debugging facilities are circuits
Debugging facilities are circuits
Observe and monitor

Take decision

You cannot watch everything
Abstract analysis: semantic needed

From information to knowledge

Signals vs Variables, etc.

Composite pattern, polymorphism, etc.
From a technical point of view

Software abstraction \[\rightarrow\text{Synthesis}\rightarrow\] Implementation in hardware

From D. Picard’s ESUG 2009 talk
Full observability isn’t scalable

Focus on POI
Full observability isn’t scalable

Focus on POI
Take control

Select your

Become a time traveller
Smalltalk debugger

- Just fit approach
- Run code and catch exception
- Code hot replacement, variable update, etc.
- Step on or resume execution
- Possible rollback

- Multiple runs
- Breakpoints update, earlier exception
- Same conceptual behavior
Dodge bullets

Once the time has stopped

... just operate!
Bullet time explained
Conditional probes

- Conditional probes offer the controllability that lacks in commercial tools.
- Observability can be gained at the cost of adding some variable look-up wires.
- ... But also using vendor’s tool such as Chipscope.
Red Pill

Decomposition

Probes

Application

Cases

Probes

Application

(Generated)

Inserted probe

Control panel

Active probes

Probes

inspector
RedPill Flow extends Biniou (HLS)

Application

High-level CDFG

Low-level CDFG

Synthesis Tools

Probed Netlist

Reconfigurable Architecture

Multi-Level Simulator

Probe Insertion
Abstract analysis

Encapsulate circuit modules as smalltalk blocks

- Enables soft and hard objects to communicate
- Delivers the power of Sunit to hardware
Abstract analysis (example)
Characterization tests & SUnit
How Many matrix?
Reboot the Matrix
Will you take the red pill?

- HLS (Biniou) offers a path from HL languages to circuits
- Vendors tools offer observability
- Red Pill offers controlability
- Object encapsulation offers abstract analysis and polymorphism.

Smalltalk debug definitely lives in the Matrix
Thank you for your attention

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